Claims

What is claimed is:

1. A method of manufacturing a closed cell trench semiconductor device, comprising:

forming a drain region;

disposing an epitaxial region over the drain region;

forming a body region over the epitaxial region;

forming a trench in first and second directions through the body region and extending into the epitaxial region, wherein the trench in the first direction and the trench in the second direction cross to form an intersection;

depositing a conductive material in the trench; and

forming a protective layer over the intersection to inhibit removal of the conductive material from the trench in and around the intersection.

2. The method of claim 1 further including the step of forming a source region in the body region adjacent to the trench.

3. The method of claim 1 further including the step of forming an oxide layer within the trench prior to depositing the conductive material in the trench.

4. The method of claim 1 wherein the trench in the first direction is substantially perpendicular to the trench in the second direction.

5. The method of claim 1 wherein the conductive material comprises polysilicon.

6. The method of claim 1 wherein the protective layer comprises photoresist.

7. The method of claim 1, wherein the drain region and the epitaxial region are doped with a first type of semiconductor material.

8. The method of claim 7, wherein the body region is doped with a second type of semiconductor material.

9. The method of claim 1, wherein the semiconductor device is a power MOSFET.

10. A method of manufacturing a semiconductor device, comprising:

forming a drain region;

depositing an epitaxial region over the drain region;

forming a body region over the epitaxial region;

forming a trench in first and second directions through the body region and extending into the epitaxial region, wherein the trench in the first direction and the trench in the second direction cross to form an intersection;

depositing a conductive material in the trench; and

removing a portion of the conductive material without forming a depression in and around the intersection of the trench.

11. The method of claim 10 further including the step of forming a protective layer over the intersection to inhibit removal of the conductive material from the trench.

12. The method of claim 11 wherein the protective layer comprises photoresist.

13. The method of claim 10 further including forming a thicker portion of conductive material over the intersection than over non-intersection areas of the trench.

14. The method of claim 10 further including narrowing a width of the trench in and around the intersection.

15. The method of claim 10 wherein the trench in the first direction is substantially perpendicular to the trench in the second direction.

16. The method of claim 10 wherein the conductive material comprises polysilicon.

17. The method of claim 10 wherein the conductive material comprises metal silicide.

18. The method of claim 10, wherein the semiconductor device is a power MOSFET.

19. In a semiconductor device comprising a trench running first and second directions through a body region, a method of inhibiting removal of conductive material from an intersection formed by the trench running in the first direction crossing the trench running in the second direction, the method comprising the steps of:

depositing the conductive material in the trench;

and

forming a protective layer over the intersection to inhibit removal of the conductive material from the trench in and around the intersection.

20. The method of claim 19 wherein the trench in the first direction is substantially perpendicular to the trench in the second direction.

21. The method of claim 19 wherein the conductive material comprises polysilicon.

22. The method of claim 19 wherein the protective layer comprises photoresist.

23. The method of claim 19, wherein the semiconductor device is a power MOSFET.

24. A method of manufacturing a semiconductor device, comprising:

forming a drain region;

depositing an epitaxial region over the drain region;

forming a body region over the epitaxial region;

forming a trench in first and second directions through the body region and extending into the epitaxial region, wherein the trench in the first direction and the trench in the second direction cross to form an intersection;

narrowing a width of the trench in and around the intersection; and

depositing a conductive material in the trench.

25. The method of claim 24 wherein the width of the trench in and around the intersection is made substantially the same as a width of the trench across non-intersection areas.

26. A semiconductor device, comprising:

a drain region;

an epitaxial region disposed over the drain region;

a body region disposed over the epitaxial region;

a trench running in first and second directions through the body region and extending into the epitaxial region, wherein the trench in the first direction and the trench in the second direction cross to form an intersection;

a conductive material deposited in the trench, wherein a protective layer formed over the intersection inhibits removal of the conductive material from the trench in and around the intersection.

27. The semiconductor device of claim 26 further including:

a source region formed in the body region adjacent to the trench; and

an oxide layer within the trench.

28. The semiconductor device of claim 26 wherein the trench in the first direction is substantially perpendicular to the trench in the second direction.

29. The semiconductor device of claim 26 wherein the conductive material comprises polysilicon and the protective layer comprises photoresist.

30. The semiconductor device of claim 26, wherein the semiconductor device is a power MOSFET.